## ABSTRACT OF THE DISCLOSURE

A memory device includes an array of flash memory cells organized as a plurality of addressable sectors, control circuitry for controlling operations on the array of flash memory cells, and a plurality of sector tagging blocks, with each sector tagging block being associated with one sector of memory cells. Each sector tagging block is adapted to generate a select signal having a first logic level when its associated sector is addressed. The sector tagging blocks are further adapted to generate a common drain signal having a first logic level when any one of the associated sectors is tagged and addressed and to generate the common drain signal having a second logic level when no addressed associated sector is tagged.